

## CLAIMS

- 1     1.     An integrated circuit fabricated by:  
2             forming a first dielectric layer in a manner that varies in the Z-dimension; and  
3             forming a first conductive layer over the first dielectric layer, the first conductive  
4 layer also varying in the Z-dimension, the first conductive layer having a length and a  
5 width, the length being substantially greater than the width, the first conductive layer  
6 being arranged in a substantially straight line along the X-dimension, and the first  
7 conductive layer comprising upper segments and lower segments, the upper segments  
8 being longer than the lower segments.
- 1     2.     The integrated circuit recited in claim 1 wherein, in forming the first dielectric  
2 layer, the first dielectric layer is arranged in a stepped manner.
- 1     3.     The integrated circuit recited in claim 1 wherein, in forming the first dielectric  
2 layer, the first dielectric layer is arranged in an undulating manner.
- 1     4.     The integrated circuit recited in claim 1 wherein, in forming the first dielectric  
2 layer, the first dielectric layer is arranged in a manner that alternates between trenches  
3 and pedestals.
- 1     5.     An integrated circuit as recited in claim 1 and further fabricated by:  
2             forming a second dielectric layer in a manner that varies in the Z-dimension;  
3             forming a second conductive layer over the second dielectric layer, the second  
4 conductive layer also varying in the Z-dimension, the second conductive layer having a  
5 length and a width, the length being substantially greater than the width, the second  
6 conductive layer being arranged in a substantially straight line along the X-dimension,  
7 and the second conductive layer comprising upper segments and lower segments, the  
8 upper segments being longer than the lower segments; and  
9             coupling the second conductive layer to the first conductive layer.

1 6. The integrated circuit recited in claim 5 wherein, in forming the second  
2 conductive layer, the upper segments in the first conductive layer are offset 180 degrees  
3 from the upper segments in the second conductive layer.

1 7. The integrated circuit recited in claim 1 wherein, in forming the first conductive  
2 layer, the first conductive layer comprises material from the group consisting of copper,  
3 aluminum, tungsten, molybdenum, titanium, gold, silver, palladium, a metal silicide,  
4 doped polysilicon, or is an alloy whose constituents are from the group.

1 8. The integrated circuit recited in claim 1 wherein, in forming the first conductive  
2 layer, the first conductive layer comprises magnetic material.

1 9. The integrated circuit recited in claim 8 wherein, in forming the first conductive  
2 layer, the magnetic material is from the group consisting of nickel-iron, cobalt-  
3 zirconium-tantalum, iron-tantalum-nickel, nickel-iron-rhenium, and ferro-silicon.

1 10. The integrated circuit recited in claim 8 wherein, in forming the first conductive  
2 layer, the magnetic material is from the group consisting of iron, nickel, cobalt,  
3 manganese, zinc, zirconium, tantalum, rhenium, silicon, and the rare earth elements, or is  
4 an alloy whose constituents are from the group.

1 11. An integrated circuit package fabricated by:  
2 forming at least one multi-level inductive element on a substrate in a serpentine  
3 pattern comprising at least two rows, wherein each row comprises upper conductive  
4 segments and lower conductive segments, and in at least one row the upper conductive  
5 segments are longer than the lower conductive segments; and  
6 mounting an integrated circuit on the substrate.

- 1 12. The integrated circuit package recited in claim 11 wherein, in forming, the upper  
2 conductive segments and the lower conductive segments are arranged in a stepped  
3 manner.
- 1 13. The integrated circuit package recited in claim 11 wherein, in forming, the upper  
2 conductive segments and the lower conductive segments are arranged in an undulating  
3 manner.
- 1 14. The integrated circuit package recited in claim 11 wherein, in forming, the upper  
2 conductive segments in one row are offset 180 degrees from the upper conductive  
3 segments in an adjacent row.
- 1 15. The integrated circuit package recited in claim 11 wherein, in forming, the at  
2 least one multi-level inductive element comprises at least one layer of magnetic material.
- 1 16. An integrated circuit component fabricated by:  
2 forming a substrate; and  
3 forming at least one multi-level inductive element on the substrate in a serpentine  
4 pattern comprising at least two rows, wherein each row comprises upper conductive  
5 segments and lower conductive segments, and in at least one row the upper conductive  
6 segments are longer than the lower conductive segments.
- 1 17. The integrated circuit component recited in claim 16 wherein, in forming the  
2 substrate, the substrate is formed of material from the group consisting of silicon,  
3 germanium, gallium arsenide, polyimide, organic material, a printed circuit board, glass,  
4 quartz, and ceramic.
- 1 18. The integrated circuit component recited in claim 16 wherein, in forming the at  
2 least one multi-level inductive element, the upper conductive segments and the lower  
3 conductive segments are arranged in a stepped manner.

1 19. The integrated circuit component recited in claim 16 wherein, in forming the at  
2 least one multi-level inductive element, the upper conductive segments and the lower  
3 conductive segments are arranged in an undulating manner.

1 20. The integrated circuit component recited in claim 16 wherein, in forming the at  
2 least one multi-level inductive element, the upper conductive segments in one row are  
3 offset 180 degrees from the upper conductive segments in an adjacent row.

1 21. The integrated circuit component recited in claim 16 wherein, in forming the at  
2 least one multi-level inductive element, the at least one multi-level inductive element  
3 comprises at least one layer of magnetic material.

1 22. An integrated circuit package fabricated by:  
2 forming a substrate;  
3 forming at least one multi-level inductive element on the substrate in a serpentine  
4 pattern comprising at least two rows, wherein each row comprises upper conductive  
5 segments and lower conductive segments, and in at least one row the upper conductive  
6 segments are longer than the lower conductive segments; and  
7 mounting an integrated circuit on the substrate.

1 23. The integrated circuit package recited in claim 22 wherein, in forming the  
2 substrate, the substrate is formed of material from the group consisting of silicon,  
3 germanium, gallium arsenide, polyimide, organic material, a printed circuit board, glass,  
4 quartz, and ceramic.

1 24. The integrated circuit package recited in claim 22 wherein, in forming the at least  
2 one multi-level inductive element, the upper conductive segments and the lower  
3 conductive segments are arranged in a stepped manner.

- 1 25. The integrated circuit package recited in claim 22 wherein, in forming the at least  
2 one multi-level inductive element, the upper conductive segments and the lower  
3 conductive segments are arranged in an undulating manner.
- 1 26. The integrated circuit package recited in claim 22 wherein, in forming the at least  
2 one multi-level inductive element, the upper conductive segments in one row are offset  
3 180 degrees from the upper conductive segments in an adjacent row.
- 1 27. The integrated circuit package recited in claim 22 wherein, in forming the at least  
2 one multi-level inductive element, the at least one multi-level inductive element  
3 comprises at least one layer of magnetic material.
- 1 28. An integrated circuit component fabricated by:  
2 forming a silicon substrate; and  
3 forming at least one multi-level inductive element on the substrate in a serpentine  
4 pattern comprising at least two rows, wherein each row comprises upper conductive  
5 segments and lower conductive segments, and in at least one row the upper conductive  
6 segments are longer than the lower conductive segments.
- 1 29. The integrated circuit component recited in claim 28 wherein, in forming the at  
2 least one multi-level inductive element, the upper conductive segments in one row are  
3 offset 180 degrees from the upper conductive segments in an adjacent row.
- 1 30. The integrated circuit component recited in claim 28 wherein, in forming the at  
2 least one multi-level inductive element, the at least one multi-level inductive element  
3 comprises at least one layer of magnetic material.
- 1 31. An integrated circuit fabricated by:  
2 forming at least one multi-level inductive element on a substrate in a serpentine  
3 pattern comprising at least two rows, wherein each row comprises upper conductive

4 segments and lower conductive segments, and in at least one row the upper conductive  
5 segments are longer than the lower conductive segments.

1 32. The integrated circuit recited in claim 31 wherein, in forming, the upper  
2 conductive segments and the lower conductive segments are arranged in a stepped  
3 manner.

1 33. The integrated circuit recited in claim 31 wherein, in forming, the upper  
2 conductive segments and the lower conductive segments are arranged in an undulating  
3 manner.

1 34. The integrated circuit recited in claim 31 wherein, in forming, the upper  
2 conductive segments in one row are offset 180 degrees from the upper conductive  
3 segments in an adjacent row.

1 35. The integrated circuit recited in claim 31 wherein, in forming, the at least one  
2 multi-level inductive element comprises at least one layer of magnetic material.